



# PTP Testing with xGenius / Zeus: IEEE 1588 - Advanced Test Option

The Precision Time Protocol (PTP/IEEE 1588) has become a foundational technology across telecommunications, power utilities, financial trading infrastructure, and industrial automation. As networks evolve to support time-sensitive workloads, rigorous validation of every node in the synchronization chain, including masters, boundary clocks, transparent clocks, and slave clocks, is no longer optional but essential.

Most PTP test instruments address only a single role at a time, either emulating a master to stimulate a device under test or a slave to analyze an incoming signal. Real networks, however, require simultaneous multi-role interaction. Validating a boundary clock (T-BC), for example, requires a coordinated upstream grandmaster and downstream slave analyzer.

The IEEE 1588 Advanced Test Option, available on the ALBEDO xGenius and Zeus platforms, resolves this limitation by enabling multi-role emulation simultaneously within a single instrument. This document describes the four testing configurations included in the option, their technical use cases, and the practical advantages they offer network operators, equipment manufacturers, and test engineers.

## 1. WHY RIGOROUS PTP TESTING MATTERS

IEEE 1588 synchronization underpins time-critical services across multiple industries:

- **Telecommunications networks (ITU-T G.8275.1 / G.8275.2):** 5G fronthaul, midhaul, and transport networks require sub-microsecond phase alignment. A non-compliant Telecom Boundary Clock (T-BC) or Telecom Time Slave Clock (T-TSC) can propagate phase errors and degrade radio performance across entire cells.
- **Power utilities (IEEE C37.238 / IEC 61850):** Protection relays and phasor measurement units (PMUs) require time accuracy better than 1 μs for correct fault detection, Sampled Values (SV) processing and synchrophasor measurement. An incorrectly synchronized IED can cause false tripping or missed faults.

- **Financial trading infrastructure:** Regulations such as MiFID II RTS 25 mandate sub-100 μs clock accuracy for trade timestamping. Failure to comply introduces both regulatory exposure and legal risk.
- **Industrial automation (IEEE 802.1AS / TSN):** Time-Sensitive Networking relies on tightly synchronized clocks to schedule traffic with deterministic latency. A misconfigured boundary clock can introduce jitter that disrupts real-time control loops.

Across these environments, testing must go beyond simple slave-analyzer configurations. Devices should be validated under conditions that reflect real network deployments, including multi-hop synchronization chains, redundant grandmaster scenarios, and asymmetric link delays.

## 2. PTP ADVANCED TEST OPTION: OVERVIEW

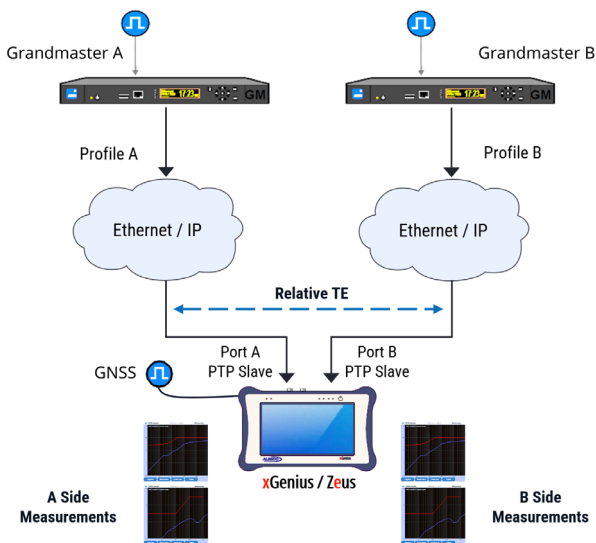
The Advanced Test Option extends the standard PTP capabilities of xGenius and Zeus with four selectable test configurations. Each configuration defines coordinated roles for Port A and Port B, and optionally Port C/PHM-25, enabling the tester to operate simultaneously as a stimulus source and a measurement analyzer for realistic validation under controlled network conditions.

**Table 1**  
Advanced PTP Test Configurations & Port Role Mapping

Config	Port A Role	Port B/C Role	Key Capability
Dual Sync Analyzer	Slave and analyzer	Slave and analyzer Port B	Dual-path TE comparison and Relative TE analysis
Dual Master Analyzer	Grandmaster (emulation)	Grandmaster (emulation) Port B	BMCA behavior, failover, and multi-domain validation
BC/TC Test	Grandmaster (emulation)	Slave and analyzer Port B	Single-unit T-BC and T-TC validation
SC Test	Grandmaster (emulation)	Clock monitor Port C / PHM-25	Physical timing output validation (TIE, TE, MTIE, TDEV)

### 3. DUAL SYNC ANALYZER

The Dual Sync Analyzer mode configures both Port A and Port B as independent PTP pseudo-slaves operating in test mode, each locking to a separate PTP master. Each port independently computes a complete set of synchronization metrics, including time error (TE), maximum time interval error (MTIE), time deviation (TDEV), packet delay variation (PDV) statistics, and clock status, all derived from its respective PTP source. The two ports can be configured with different PTP profiles, addressing modes, or transport mechanisms, enabling the simultaneous evaluation of dissimilar network segments.



**Figure 1** Dual Sync Analyzer measuring TE on two independent PTP paths and their Relative TE.

A key capability of this mode is the measurement of Relative Time Error (Relative TE), defined as the difference between the absolute TE observed at Port A and Port B. Because this metric inherently cancels out correlated error sources, such as reference clock instability, it can be obtained without requiring an external GNSS or 1PPS reference. This makes the Dual Sync Analyzer mode particularly effective for comparing synchronization performance across independent paths in scenarios where an absolute time reference is unavailable or impractical to deploy.

#### Applicable Standards and Metrics

- ITU-T G.8271.2: TE budget for partial timing support scenarios
- ITU-T G.8273.2: T-BC characterization across parallel network paths
- IEEE C37.238: Parallel PTP path comparison in redundant substation topologies
- ITU-T G.8260: pktFilteredMTIE and pktFilteredTDEV measurements on both ports

### Real-World Use Cases

#### Use Case 1: Active / Standby GM Path Comparison

In telecom networks with active and standby PRTC/T-GM paths, it is essential to verify timing equivalence before switchover. Port A locks to the active path and Port B to the standby path. The resulting Relative TE provides a real-time comparison without requiring a local GNSS reference. A near-zero Relative TE confirms readiness for seamless switchover.

#### Use Case 2: Asymmetric Link Delay Detection in Redundant Networks

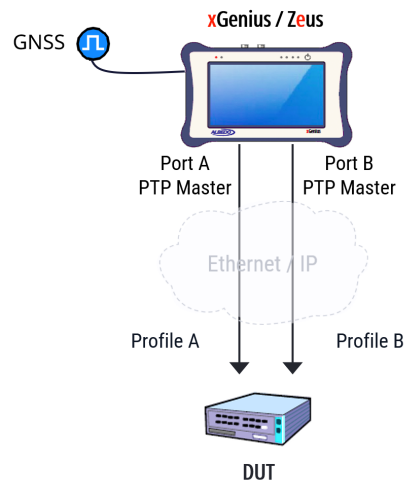
Asymmetric delays in redundant networks can degrade PTP accuracy. By connecting Port A and Port B at different points in the network, the tester isolates path-specific asymmetry using Relative TE. This approach removes common-mode effects and directly quantifies the TE contribution of the suspect segment.

#### Use Case 3: Multiple-Profile PTP Validation

Multiple PTP profiles, such as ITU-T G.8275.1 and G.8275.2, can be validated concurrently. Port A and Port B are configured independently, allowing parallel measurement of TE, MTIE, and TDEV for each domain. This confirms correct operation without cross-domain interference while reducing overall test time.

### 4. DUAL MASTER ANALYZER

The Dual Master Analyzer mode configures Port A and Port B as independent PTP grandmaster emulators, each generating a fully characterized master signal with configurable clock attributes, including Clock Class, Clock Accuracy, PTP Variance, Priority 1/2, domain, and relative time offset. Both instances operate independently and can inject different or conflicting clock qualities to evaluate device behavior under controlled conditions.



**Figure 2** Dual Master Analyzer generating two independent PTP profiles towards a DUT.

This mode is designed to validate PTP operation in multi-master environments, including BMCA selection, redundancy schemes, master failover, and domain separation. It also supports testing of PTP-aware switches and routers, ensuring correct handling of announce messages in accordance with the configured profiles. Configurable time offsets between the two grandmaster instances enable validation of slave clock behavior under timing divergence and controlled switchover scenarios.

## Applicable Standards and Metrics

- *IEEE 1588-2019 § 9*: Best Master Clock Algorithm (BMCA) state machine
- *ITU-T G.8275.1*: Telecom profile announce message handling and priority hierarchy
- *ITU-T G.8275.2*: unicast master selection and failover
- *IEEE C37.238*: Redundant grandmaster testing for substation automation
- *IEEE 802.1AS*: BMCA testing for TSN / automotive Ethernet bridges

## Real-World Use Cases

### Use Case 1: BMCA Convergence and Validation

PTP-capable switches must correctly execute the Best Master Clock Algorithm when multiple masters are present. Using Dual Master Analyzer mode, Port A is configured with higher clock quality (e.g., Clock Class 135) and Port B with lower quality (e.g., Clock Class 165). Both connect simultaneously to the DUT. The engineer verifies correct master selection, expected port states (MASTER/PASSIVE), and exercises edge cases by modifying Priority and clock attributes.

### Use Case 2: Grandmaster Failover Testing

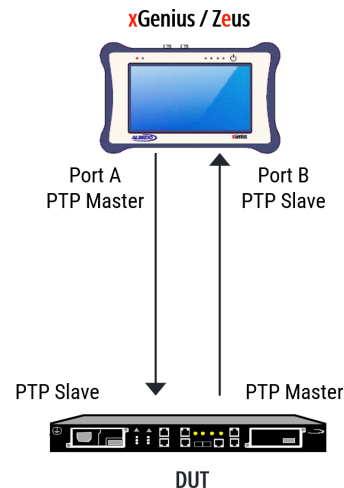
In telecom networks, slave clocks must re-lock to a standby master within a defined interval after failure of the active source. Port A operates as the active grandmaster and Port B as standby. After lock is established, Port A is disabled. The time from the last Announce message to the DUT's transition to the new SLAVE state is measured, confirming compliance with failover timing requirements.

### Use Case 3: Slave Clock Timing Divergence Tolerance

Redundant grandmasters may exhibit small phase differences during holdover, failover, or GNSS degradation. Port A and Port B are configured as independent grandmasters with a controlled relative time offset. By progressively increasing the offset between both masters, engineers can evaluate the DUT's tolerance to timing divergence and verify its behavior under non-ideal synchronization conditions.

## 5. BC/TC TEST

In BC/TC test mode, Port A of the xGenius or Zeus operates as a PTP grandmaster, providing a controlled timing reference to the device under test (DUT), while Port B acts as a PTP pseudo-slave, measuring the signal at the DUT output. Port B computes synchronization metrics including Time Error (TE), MTIE, TDEV, and PDV based on the received PTP stream.



**Figure 3** Boundary Clock (BC) and Transparent Clock (TC) clock qualification.

Because both ports share the same internal oscillator, and optionally the same external reference, correlated error sources cancel, improving overall measurement accuracy compared to multi-instrument setups. While an external reference such as GNSS or a PRTC enhances traceability, the test can be performed using the internal oscillator alone, making it well suited for lab and production environments.

## Applicable Standards and Metrics

- *ITU-T G.8273.2*: T-BC and T-TSC noise generation, noise tolerance, transient response
- *ITU-T G.8271.1*: TE budget at reference point C
- *IEEE C37.238*: BC qualification for power substations
- *IEC 61850-9-3*: Merging unit time synchronization in protection applications
- *IEEE 802.1AS*: BC testing in TSN environments

## Real-World Use Cases

### Use Case 1: 5G Transport Network T-BC Certification

Telecom Boundary Clocks in 5G transport networks must comply with ITU-T G.8273.2 noise generation limits. Port A provides the PTP grandmaster reference to the T-BC, while Port B measures the resulting TE at the output. Automated dTE (Class A/B) mask comparison

determines compliance. The single-unit setup eliminates the need for synchronized multi-instrument deployments.

### Use Case 2: TC Insertion Delay Verification

Transparent Clocks must accurately compensate for packet residence time. Port A injects a PTP stream into the TC, while Port B captures the forwarded traffic. The tester verifies correction field updates and detects timestamping inaccuracies as residual TE at the output.

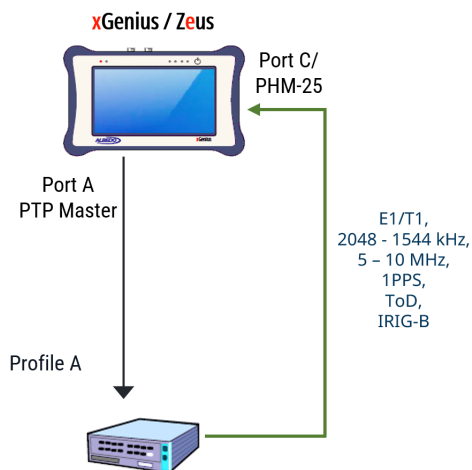
### Use Case 3: PTP Profile Translation BC Testing.

During substation commissioning, a Boundary Clock receives time from a telecom PTP profile, such as ITU-T G.8275.1 or G.8275.2, and redistributes it to protection and automation devices using IEEE C37.238 Power Profile or IEC/IEEE 61850-9-3 Utility Profile. Port A emulates the upstream telecom-profile Grandmaster, while Port B analyzes the translated output and verifies compliance with applicable IEC/IEEE 61850-9-3 or G.8273.2 Class A TE limits.

## 6. SC TEST

The Slave Clock (SC) test mode is intended for PTP slave clocks with physical timing outputs, such as 1 PPS, Time-of-Day (ToD), frequency signals (e.g., 2.048 MHz, 10 MHz), or IRIG-B. This configuration applies to DUTs that distribute recovered time through dedicated timing interfaces.

In this mode, Port A of the xGenius or Zeus operates as a configurable PTP grandmaster, providing the IEEE 1588 input to the DUT. Port C receives the physical output and measures synchronization metrics, including TIE, TE, MTIE, and TDEV, against the instrument reference. When equipped with a PHM-25 module, Port C can also analyze IRIG-B signals, extending compatibility to a wider range of timing devices.



**Figure 4** Slave Clock (SC) Test Configuration for Physical Output Validation.

## Applicable Standards and Metrics

- *ITU-T G.8272 / G.8272.1*: PRTC-A and PRTC-B / ePRTC noise generation limits
- *ITU-T G.8273.4*: T-GMCS noise generation (integrated GNSS grandmaster clocks)
- *ITU-T G.810 / G.8260*: TIE, TE, MTIE, TDEV definitions and pktFiltered variants
- *IEC 61850-9-3 / IEEE C37.238*: 1PPS output timing for protection relays
- *IRIG-B*: Time code verification via PHM-25 module

## Real-World Use Cases

### Use Case 1: Grandmaster 1PPS Output Qualification

Before commissioning a GNSS grandmaster (PRTC), operators must verify that its 1PPS output meets ITU-T G.8272 PRTC-A limits independently of GNSS. Port A provides a controlled PTP reference, while Port C measures the 1PPS output against the instrument's reference. MTIE and TDEV analysis confirms compliance, validating the DUT's internal servo and holdover performance.

### Use Case 2: Industrial Controller Time Accuracy Verification

Industrial controllers often rely on a 1PPS output for time-triggered processes. Using SC test mode, Port A injects a controlled PTP signal and Port C measures the 1PPS output. Time Error is monitored against the 1  $\mu$ s end-to-end accuracy requirement of IEEE 802.1AS-2020 Annex B.3 over extended tests, with MTIE and TDEV revealing convergence behavior, overshoot, and holdover performance.

### Use Case 3: ToD Accuracy for Network Time Applications

Network time appliances used in financial environments must deliver accurate ToD signals for time-stamping. With ToD input on Port C, the tester verifies that the generated time meets regulatory accuracy requirements. The test also confirms correct UTC offset and leap second handling, which are critical for compliance audits such as MiFID II.

## 7. TEST CASE QUICK-REFERENCE MATRIX

The following matrix maps common network testing scenarios to the appropriate Advanced Test configuration, helping test engineers select the right mode before starting a test campaign.

**Table 2**  
Test case quick reference matrix

Test Scenario	Configuration	DUT Type	Key Metrics
Active/standby GM path comparison	Dual Sync Analyzer	Network / DUT agnostic	Relative TE, MTIE/TDEV both ports
Fiber asymmetry quantification	Dual Sync Analyzer	Network path	Relative TE, PDV asymmetry
Multi-profile PTP switch validation	Dual Sync Analyzer	Multi-profile PTP switch	TE per profile
BMCA master election correctness	Dual Master Analyzer	PTP switch / slave	Port state, election time
Grandmaster failover time measurement	Dual Master Analyzer	T-BC / T-TSC	Failover time, announce timeout
PTP domain isolation / leakage detection	Dual Master Analyzer	Multi-domain switch	Domain mismatch counters
T-BC noise generation (G.8273.2 Class A/B)	BC/TC Test	Telecom Boundary Clock	TE, dTE, MTIE/TDEV mask
Transparent clock residence time correction	BC/TC Test	PTP Transparent Clock	Correction field accuracy, TE
Substation BC Profile Translation	BC/TC Test	Substation BC	cTE < 50 ns, PDV, MTIE
Grandmaster 1PPS output (PRTC-A mask)	SC Test	T-GM / PRTC	TIE, TE, MTIE/TDEV G.8272 mask
Slave clock 1PPS output quality	SC Test	T-TSC, Slave Clock	TE, MTIE, TDEV, holdover
ToD signal accuracy (MiFID II compliance)	SC Test	Network Time Appliance	TE < 100 $\mu$ s, UTC offset

## 8. CONCLUSION

PTP synchronization networks are increasingly complex, requiring validation under stringent multi-role and multi-path conditions. The IEEE 1588 Advanced Test Option on the ALBEDO xGenius and Zeus platforms provides four complementary configurations that cover the full range of PTP devices and scenarios:

- **Dual Sync Analyzer:** Dual-path monitoring with reference-free Relative TE
- **Dual Master Analyzer:** BMCA, failover, and multi-domain validation
- **BC/TC Test:** Single-unit Boundary and Transparent Clock qualification
- **SC Test:** Physical timing output validation (1PPS, ToD, frequency)

Together, these configurations reduce instrument count, shorten test time, and improve measurement accuracy through the shared oscillator and reference architecture of the xGenius and Zeus platforms.